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PATENT & TRADEMARK OFFICE

DECLARATION

As a below-named inventor, I declare that:

my residence, post office address, and citizenship are as stated next to my name;

I believe that I am an original and first inventor of the invention entitled "Semiconductor Integrated Circuit Device Comprising Synchronous DRAM Core And Logic Circuit Integrated Into A Single Chip And Method Of Testing The Synchronous DRAM Core" described and claimed in the attached specification;

I have reviewed and understand the contents of the specification, including the claims, as amended by the Preliminary Amendment filed June 4, 2001 and the Amendment concurrently filed;

I acknowledge the duty to disclose information that is material to the examination of this application in accordance with 37 C.F.R. §1.56(n); and

I hereby claim foreign priority benefits under Title 35, United States Code §119 of the foreign application for patent listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application from which the benefit of priority is claimed.

Prior Foreign Application

(Number)	(Country)	(Day/Month/Year Filed)
9-086600	Japan	04/04/97

United States Patent 5,910,181, which matured from United States Patent Application Serial Number 08/964,236, is partly inoperative or invalid by reason of claiming less than I had a right to claim based on the disclosure of the patent application. The patent application disclosure does not limit the invention to a synchronous dynamic random access memory but discloses the invention as pertaining to other kinds of random access memory particularly as described at column 13, lines 62-65 of United States Patent 5,910,181. In addition, minor errors of a grammatical or typographical nature appear in claims 1-3, 5, 6, 7, and 9 of U. S. Patent 5,910,181.

To the best of my knowledge, the errors occurred without deceptive intent. Correction of the errors is sought by correcting claims 1-3, 5, 6, 7, and 9 and by adding claims 10-18 as shown in the attached papers.

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As a named inventor, I hereby appoint Leydig, Voit & Mayer to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Customer Number 23548.

23548

I further direct that correspondence concerning this application be directed to Leydig, Voit & Mayer: Customer Number 23548.

23548

I declare that all statements made here based on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of this reissue patent application or any reissued patent issuing from this application.

Full name of **sole or first inventor:** Makoto HATAKENAKA

Inventor's signature Makoto Hatakenaka

Date December 1, 2003 Country of Citizenship: Japan

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Full name of **second joint inventor,** if any: Akira YAMAZAKI

Inventor's signature Akira Yamazaki

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Full name of **third joint inventor,** if any: Shigeki TOMISHIMA

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Date December 9, 2003 Country of Citizenship: Japan

Residence: Tokyo, Japan
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Full name of **fourth joint inventor,** if any: Tadato YAMAGATA

Inventor's signature Tadato Yamagata

Date December 1, 2003 Country of Citizenship: Japan

Residence: Tokyo, Japan
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